



ManpowerGroup is a worldwide innovative forerunner and leader in the field of employment through the provision of services and workforce management solutions for clients and helping people in their career development with the aim of understanding the needs of the clients and candidates in the changing world of work.

On behalf of our client, a global supplier of micro-electronic semiconductor solutions, we are looking for intelligent and independent candidate to fulfil the position of:

## Senior Analog Design Engineer / Team Lead

*(Location: Sofia, Bulgaria)*

### **Brief Description:**

Create the required design and related documentation of a complete product to contribute to the achievement of the projects' targets in terms of product specification, cost, quality and timing. Ensure that all people management processes and related practices are professionally implemented with a special emphasize in optimizing the learning through developing and coaching the team members in their assigned projects.

### **Candidate profile:**

#### **Concept / Top Level Design**

Support in building of the top-level concept design. Modelling of building blocks. Support in creating and maintaining the specifications

- ✓ Knowledge of specific methods and tools to implement models for building blocks present in
- ✓ high complexity projects:
- ✓ For high complexity projects, have conceptual knowledge of the full design, including digital, memories, sensor models.
- ✓ Able to challenge and support SA on sub-systems and full chip specifications.
- ✓ Able to perform risk assessment on top level.

## Top Level Simulation

Setup of the relevant testbenches needed to simulate the full chip top level schematic. Verification of the specified functions of the design. Assessment of the acquired simulation results.

- ✓ Create testbenches needed for full chip validation.
- ✓ Be able to identify and assess the critical parameters in a design.

## Lead designer:

- ✓ Knowledge to decide on list of required simulations on block, analog-top and full top level.
- ✓ Able to assess top level functionality.
- ✓ Able to critically analyze testbenches and simulation results obtained by another designer on the same project.

## Design Implementation

Knowledge of design concepts. Knowledge of simulation techniques and other tools needed to verify the block level design. Awareness of guidelines and specifications regarding design implementation.

- ✓ Be able to implement high complexity analog building blocks while taking into account all external influences.
- ✓ Knowledge of the requirements of other sub-processes on the design implementation (DFx):
- ✓ Examples:
  - Design for reliability,
  - Design for test,
  - Design for FA...
- ✓ Understanding of ESD and EMC, know and follow and give feedback on guidelines regarding both issues.
- ✓ Knowledge of existing simulation models and their limitations (i.e. High voltage transistor models, L/W for resistors...).
- ✓ Know, follow and give feedback on guidelines regarding naming, hierarchy, design checklists... to assure efficient design reuse.
- ✓ Knowledge of advanced cadence simulations.
- ✓ Able to estimate design time needed for blocks present in high complexity projects.

## Design Review

Be able to critically review designs done by another designer and propose technical solutions if needed.

- ✓ Able to analyze and find critical design parameters in a design done by another designer on another project.
- ✓ Active Knowledge (able to implement in practice) of lessons learned and design review checklist items.
- ✓ Challenge other DE's on performed simulations and the acquired results.

- ✓ Able to suggest and actively contribute lessons learned, based on the performed design review.

### **Layout and back annotation**

Knowledge of layout parasitics and how to simulate them. Awareness of layout constraints and resulting design limitation.

- ✓ Be able to simulate a schematic including layout extracted parasitics.
- ✓ Advanced knowledge of technology and parasitics.
- ✓ Knowledge of external factors influencing floorplan and top level layout (grounding strategy, temperature gradients...).
- ✓ Knowledge of Design Rules impacting top level layout and floorplan.
- ✓ Able to estimate area of blocks at concept design.
- ✓ Know, follow and provide feedback guidelines regarding ESD and EMC.
- ✓ Able to define layout constraints and supervise the layout integration.

### **Documentation**

Able to document the needed information in a thorough way according to design standards.

- ✓ Know which information to document and report.
- ✓ Know which template to use.
- ✓ Know where to store this information.
- ✓ Contribution to creation and improvement of the required templates/guidelines.
- ✓ Able to fill the required documents in a structured and timely fashion.

### **Test**

Support test group in implementing a time/cost-efficient automatic testing. Design and verification of the “Design for Testability”. Be able to implement the required testability on top level.

- ✓ Be able to estimate specs for parameters relevant to top level performance.
- ✓ Able to provide support during debugging and able to analyze potential critical failures of the implemented test interface.
- ✓ Basic knowledge of test infrastructure.
- ✓ Evaluate test related items (RnR, CGM, CPK...) and able to suggest possible redesign improvements.

### **Product Characterization (ESR)**

Creation of characterization plan. Support/do the measurements. Analysis of the measurement results and conclusions.

- ✓ Be able to create the characterization plan for high complexity project.

- ✓ Be able to make assessment on needed efforts and duration. Be able to set requirement to characterization HW.
- ✓ Be familiar/able to perform bench measurement with standard lab equipment.
- ✓ Able to correctly interpret the characterization results and take necessary containment or corrective actions in to guarantee a successful redesign at smallest cost.
- ✓ Transfers relevant results to dedicated lessons learned.
- ✓ To be able to define Product Reliability tests.

### **Failure Analysis**

Analyse and debug ICs and support of FA and Q engineers. Interpreting of the results.

- ✓ Able to analyze and debug complex IC's.
- ✓ Know standard and application specific evaluation tools (IC-testers, measurement equipment, microprobing, qualification and characterization...).
- ✓ Able to support the Quality Engineer during the evaluation of the fails (customer returns).
- ✓ Able to interpret the results and to take the appropriate conclusion in terms of root cause and containment/corrective actions.
- ✓ Able to lead FA strategy and debug full chip.
- ✓ Act as interface to communicate the FA results to other projects or teams (if relevant).

### **Project release**

Support product qualification / PPAP. Analysis of statistical results.

- ✓ Knowledge of qualification requirements and standards.
- ✓ Contribute to the creation of qualification setup (HTOL, burn-in, etc.).
- ✓ Knowledge of statistical methods as CPK, RnR in order to support test and qualification from design point of view.
- ✓ Drive required CPK analysis and yield improvement actions.

### **Required skills:**

- ✓ Master in micro-electronics, above 5 years of related experience as designer in a micro-electronics environment
- ✓ Fluency in English is a must. Knowledge of any major European / Asian language is a strong asset
- ✓ Successful experience in managing a design team (people leadership, resource allocation)
- ✓ Working experience in integrating different cultural backgrounds
- ✓ Working experience in International Industry
- ✓ Working experience in Automotive Industry

- ✓ Medium Travel Intensity
- ✓ Working experience in managing virtual teams
- ✓ Successful track record for design of automotive projects
- ✓ Working experience Exp w/ remote teams

## The selection process is taking place NOW!

If you consider yourself appropriate for this position, we invite you to apply for the position through our website

**[www.manpower.rs](http://www.manpower.rs) , Job Order 1839**

Deadline for applications: /

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All applicants will be informed and shortlisted candidates will be invited for an interview.